Honeywell

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LCSP MOS
FAULT DIAGNOSIS

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FAULT DIAGNOSIS

7.1 INTRODUCTION

This fault diagnosis procedure is aimed to supply an isolating guide for the faults with fixed symptom which firstly are attributed to the LCSP subsystem, MOS Model.
The procedure isolates the faults at component level for the Power Supply area, at board level for the logics and at component/assembly level for the mechanics.
Should the error persist also after the isolation of a faulty component, it is necessary to restart the procedure after having replaced the isolated component. Furthermore it is necessary that the supply voltage (VAC) does not exceed the allowed tolerance limits (+10%/-15%) during execution of the procedure.
Implementation of this procedure does not require a specific knowledge of the unit, but only a general knowledge of the used symbols and of the electronic components functioning.
Needed Material:

- Personal F.E. tools kit
- Unit documentation (Product Manual)

The needed spare parts are available at the District depots, exception made for the transformer, which however it is very difficult to break down.

7.2 MAINTENANCE POLICY

The current "maintenance policy" of the LCSP MOS printer foresees the faulty part isolation with the unit in off line.
The possible presence of the "on line" diagnostics, supplied by the system which the LCSP is connected to, is only useful for a check-out of the connection without giving an automatic isolation.

Before describing the suggested replacement level (board, chip, etc.) and the media supplied for this purpose, remember that as from November 1977 the LCSP (*) could be optionally supplied with a special diagnostic (resident in the printer and therefore possible to start-up in local) which will give the automatic isolation of the faulty part (Refer to para 7.3 for its description).
This performance cannot be retrofitted because the LCSP manufactured up-to-now are not preset for it.
Therefore the fault diagnosis flows will show different branches whether the unit under study is or not supplied with the above diagnostic.

Apart from the repair media available, the foreseen replacement level (supported by the spare part kits) is the following:

Logics : CPU board (without EPROM), EPROM chip (firmware), Keyboard (assembly) or key; 1000 feet board (option), L00CU board (Option); CPO board (without EPROM) for LINA 2X model

Analogic : DRIVE board (Option); VFU components (option), i.e.: motor, lamp, optic prism, plate;

Mechanic : Paper or carriage STEP motor; head assembly; various parts (belts, microswitches, mistor etc.);

Power Supply : Components (diode parts, capacitors, etc.).

All LCSP printers may either print the graphic set in LOCAL (by pressing LOCAL-TEST-START buttons) or perform some carriage movements without printing (by pressing LOCAL-TEST-LOCAL buttons).
These functions are always performed at 120 cps whenever be the LCSP speed level.

(*) The SARA model LCSP to be used as terminal and console printer can undergo a delay of two or three months on the above date.

7.3. AUTOMATIC DIAGNOSTIC

The internal diagnostic routines automatically perform the fault isolation on:

- CPU Board (CPO for LINA model)
- EPROM chip (firmware)
- RAM chip (memory)
- line (internal circuit)

In case of OK symptom, the fault is to be traced on the LINE, on the DRIVE board or on the MECHANICS (the options are not controlled by this diagnostic).
The discrimination between DRIVE and MECHANICS fault is supplied by the fault isolation flow.

The diagnostic routines are contained in a chip (EPROM) mounted on the CPU board or, should the firmware EPROM chips occupy all free positions, they are inserted on a board (AFFD) to be installed on the standard logic module.
In case the LCSP has the AFF option (front inserter), the chip will be mounted on the AFF board of the option itself.
A connector is supplied for the line check-out.
This connector is to be inserted in place of the modem cable in the printer output.

TYPE OF LCSP	DIAGNOSTIC CHIP POSITION	DIAGNOSTIC OPTION COMPONENTS	DIAGNOSTIC OPTION IPI
SARA 2 X	Free Socket on PWA CPU	1 EPROM, 1 line connector	GTWF 309A
ROSY 26 POLY 21	Side Socket on AFFD board (U01)	1 EPROM, 1 line connector	GTWF 309A
ROSY 24 with AFF ROSY 26 with AFF	Side Socket on AFF board (U01)	1 EPROM, 1 line connector	GTWF 309A
POLY 21 with AFF	Side Socket on AFF (U01) board in place of the "F/W AFF" EPROM chip which must be removed during the operability test.	1 EPROM, 1 line connector	GTWF 309A
ROSY 24 B	Side Socket on AFFD board (U01)	1 EPROM, 1 line connector, 1 AFFD board, 1 cable	GTWF 309B

7.4 AC AND DC VOLTAGES - OK CONDITION

The following figure shows the AC and DC voltages values with unit operational (breaker ON but without printing) and the pertinent points on which to perform the Ohmmeter check.

POWER SUPPLY

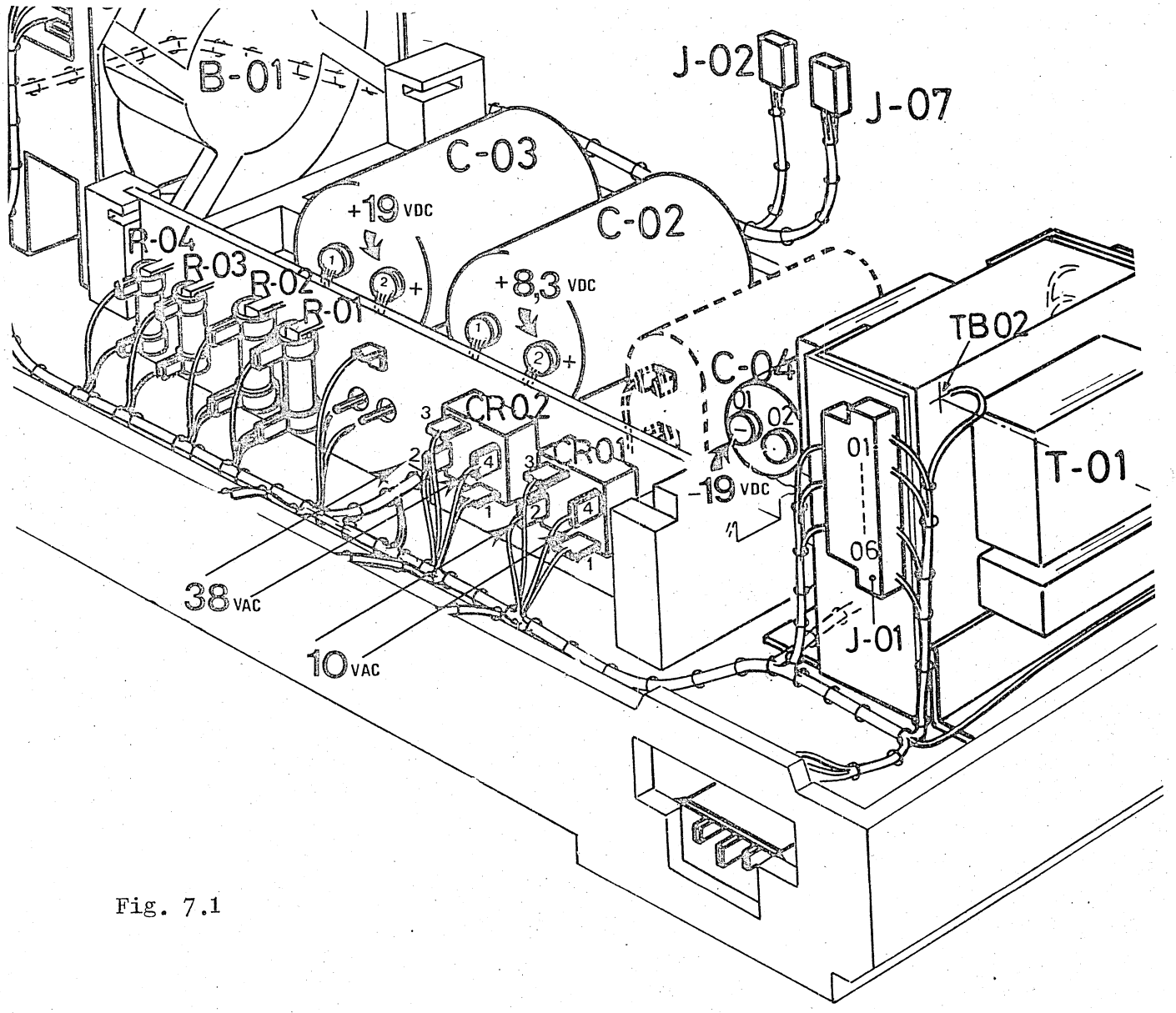

Fig. 7.1

DRIVE BOARD :

C20 Capacitor + = + 12 VDC regulated (derived from + 19V)
C22 capacitor - = - 12 VDC regulated (derived from -19 V)
C73 capacitor + = + 5 VDC regulated (derived from +8.5 V)
C14 capacitor - = - 5 VDC regulated (derived from - 19V)
C74 capacitor - = - 15 VDC regulated (derived from -19 V)

The physical position of the capacitors must be traced by referring to the "PWA DRIVE" drawing bearing the same revision level of the board under examination (see the General Index of the Volume).

From Page 7.7

B

The diagnostic operating messages are monitored through the operator panel lamps. Refer to the following symbology for a correct interpretation:

- LAMP OFF
- LAMP ON
- LAMP FLASHING

Seeing as though the lamps are differently set in the various model operator panels, in the symbology the positions of the lamps are indicated with A – B – C letters.
The correspondence between lamps, models and letters is the following:

SARA :	A = LOCAL	B = READY	C = ST. BY
ROSY :	A = LOCAL	B = ONLINE (READY)	C = ST. BY
POLY :	A = LOCAL	B = CALL	C = ST. BY

The only difference is the position of the lamp identified with letter B.

TRIP THE BREAKER OFF. HOLD TEST BUTTON PRESSED AND SIMULTANEOUSLY TRIP THE BREAKER ON.

A B C

Indication of diagnosis procedure start-up for 20 sec. approx. (The simultaneous flashing of the three lamps is also used as LAMP TEST indication).

THE FIRST PART OF THE T&D PERFORMS THE CPU (or CFO) BOARD, EPROM AND RAM CHIPS DIAGNOSIS

HAS AN ERROR BEEN DETECTED ON THE PART OF LOGIC ALREADY VERIFIED ?

YES → FAULT INDICATION. REFER TO THE DICTIONARY ON PAGE 7.10

NO

A B C

Indication of WAIT for the line test for 20 sec. approx. The special plug must be mounted on the line connector when having to check the line functioning before the TEST start-up

IS THE LINE TEST TO BE PERFORMED ?

YES → PRESS TEST BUTTON DURING WAIT INDICATION

NO

MONITORING FOR 20 SEC. OF THE FINAL SYMPTOM WHICH CAN BE EITHER

1) OK SYMPTOM A B C

Logic part operational. In this case the fault is either on the DRIVE board or on the mechanics (Motors Head,.....). Restart the procedure as from step C on page 7.7

or

2) FAULT SYMPTOM: See Dictionary on page 7.10

7.6 ERROR SYMPTOMS DICTIONARY

A	B	C	PART TO BE REPLACED
⊗	⊗	⊗	Replace the CPU (or the CPO) board
○	⊗	●	Replace the CPU (or the CPO) board
○	○	⊗	Replace RAM chips fitted in positions U02 and U07 of PWA CPU
○	⊗	○	Replace RAM chips fitted in positions U01 and U06 of PWA CPU
○	⊗	⊗	Replace RAM chips fitted in positions U04 and U09 of PWA CPU
⊗	○	○	Replace RAM chips fitted in positions U03 and U08 of PWA CPU
⊗	○	⊗	Replace RAM chips fitted in positions U05 and U10 of PWA CPU
●	○	⊗	Replace EPROM chip fitted in position U14 of PWA CPU
●	⊗	○	Replace EPROM chip fitted in position U15 of PWA CPU
●	⊗	⊗	Replace EPROM chip fitted in position U16 of PWA CPU
●	⊗	●	Replace EPROM chip fitted in position U17 of PWA CPU
●	●	⊗	Replace EPROM chip fitted in position U21 of PWA CPU
⊗	⊗	○	C Generic Fault. As first operation, it is advisable to replace the CPU or the CPO board
○	●	⊗	
⊗	○	●	
⊗	●	○	
⊗	●	●	
○	○	⊗	
○	●	○	
○	●	●	
●	○	○	
●	○	●	
●	●	○	
●	●	●	